



*Approved*

FIG.1a

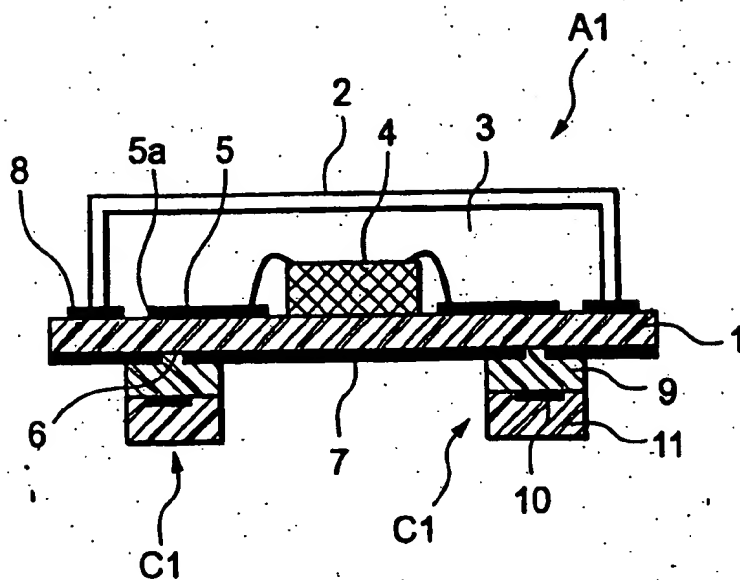
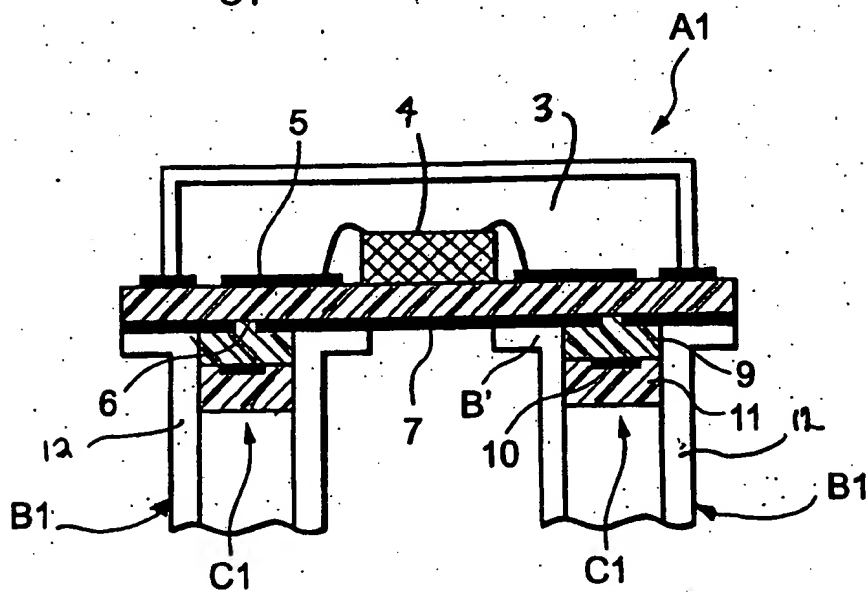


FIG.1b



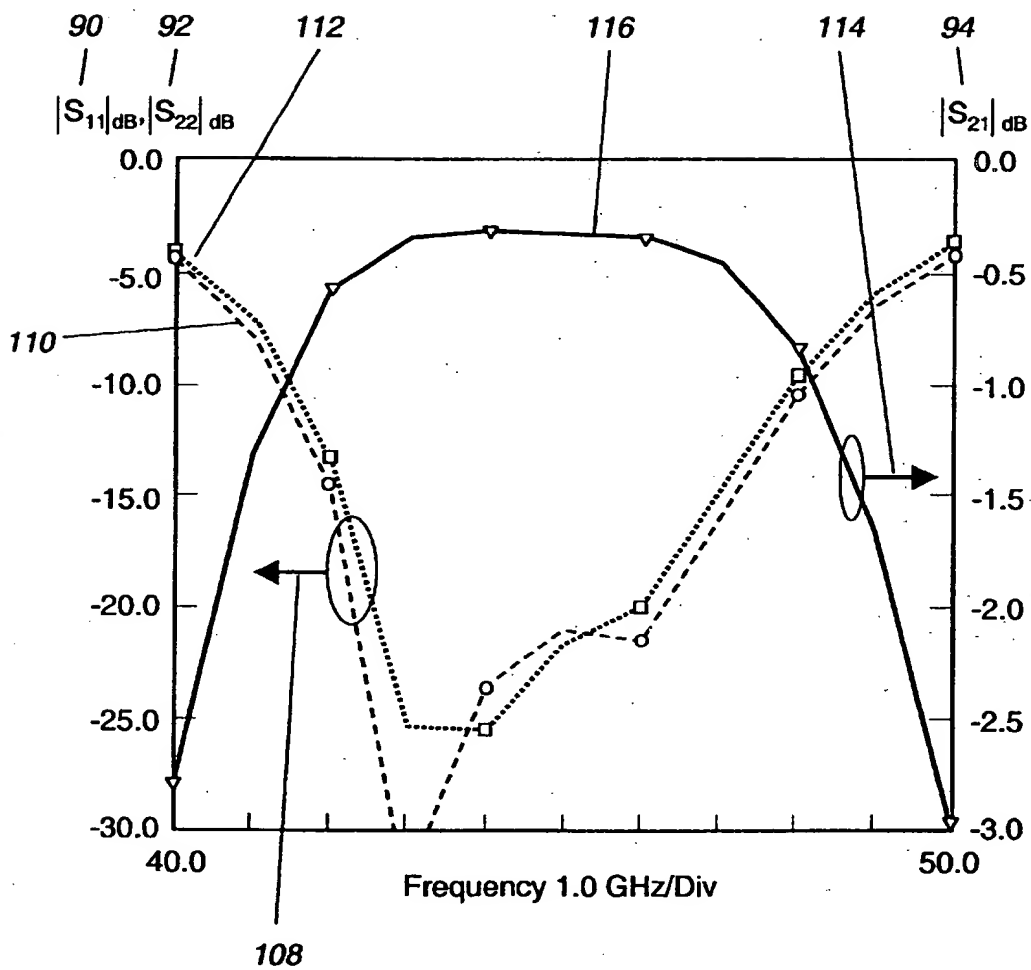


Figure 6

A cross-sectional view of a semiconductor device. A central gate structure (4) is positioned on a substrate (1). The gate structure is flanked by two regions (5) and (8). Below the gate structure, there are two regions (10) and (17). The device is connected to a common terminal (C2) and a gate terminal (A2). The substrate (1) is shown with a cross-hatched pattern. The gate structure (4) is shown with a diagonal hatched pattern. The regions (5) and (8) are shown with a solid pattern. The regions (10) and (17) are shown with a diagonal hatched pattern. The common terminal (C2) is shown with a cross-hatched pattern. The gate terminal (A2) is shown with a solid pattern.

[illegible]

This cross-sectional view shows a semiconductor device with a central gate structure. The gate structure consists of a central gate layer (7) and side gate layers (13a) on either side. The side gate layers (13a) are connected to a common gate terminal (A2) at the top. The device is supported by a substrate (B1) with a top layer (B'). The substrate has a central opening (C2) and side openings (C2) on either side. The side openings (C2) are connected to a common contact terminal (B1) at the bottom. The central opening (C2) is also connected to a common contact terminal (B1) at the bottom. The device is shown in a cross-sectional view with various layers and structures labeled with reference numerals.

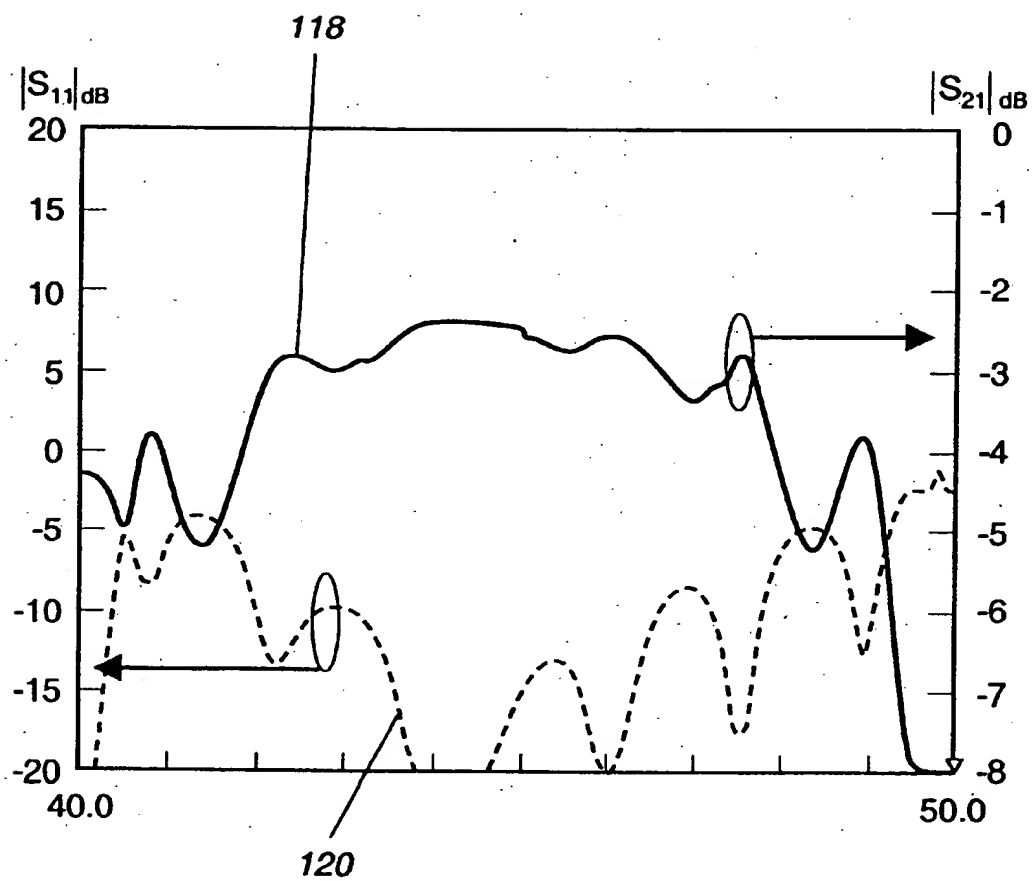


Figure 7



FIG.4a

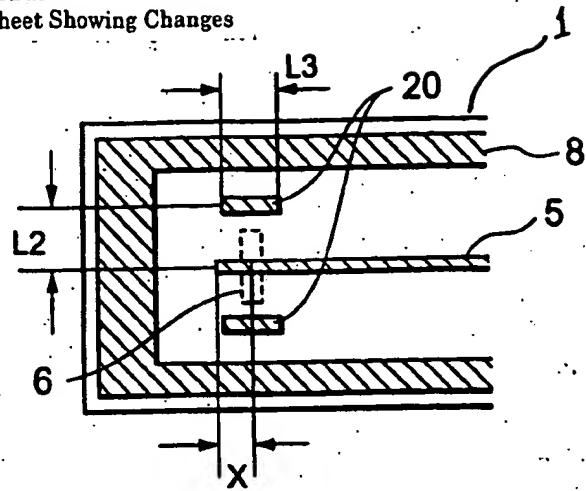


FIG.4b

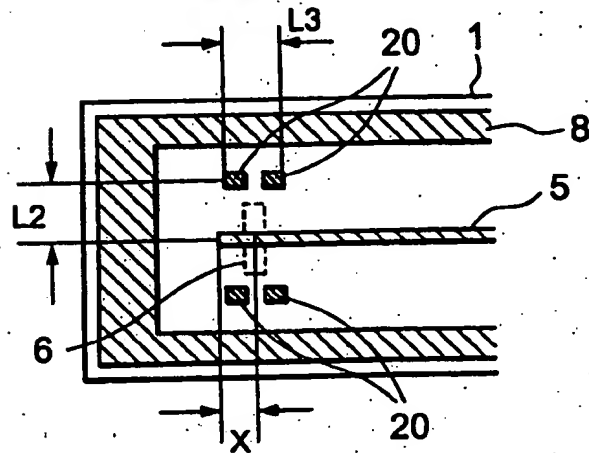


FIG.4c

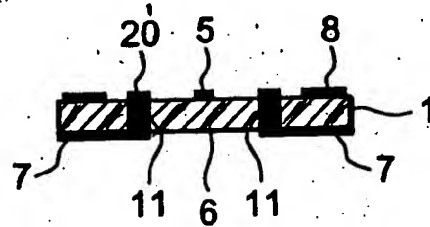


FIG.4d

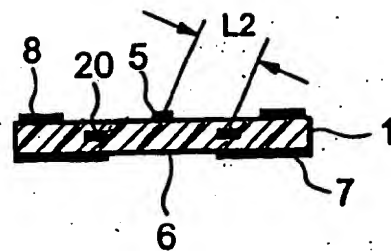
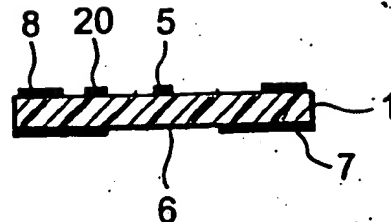


FIG.4e



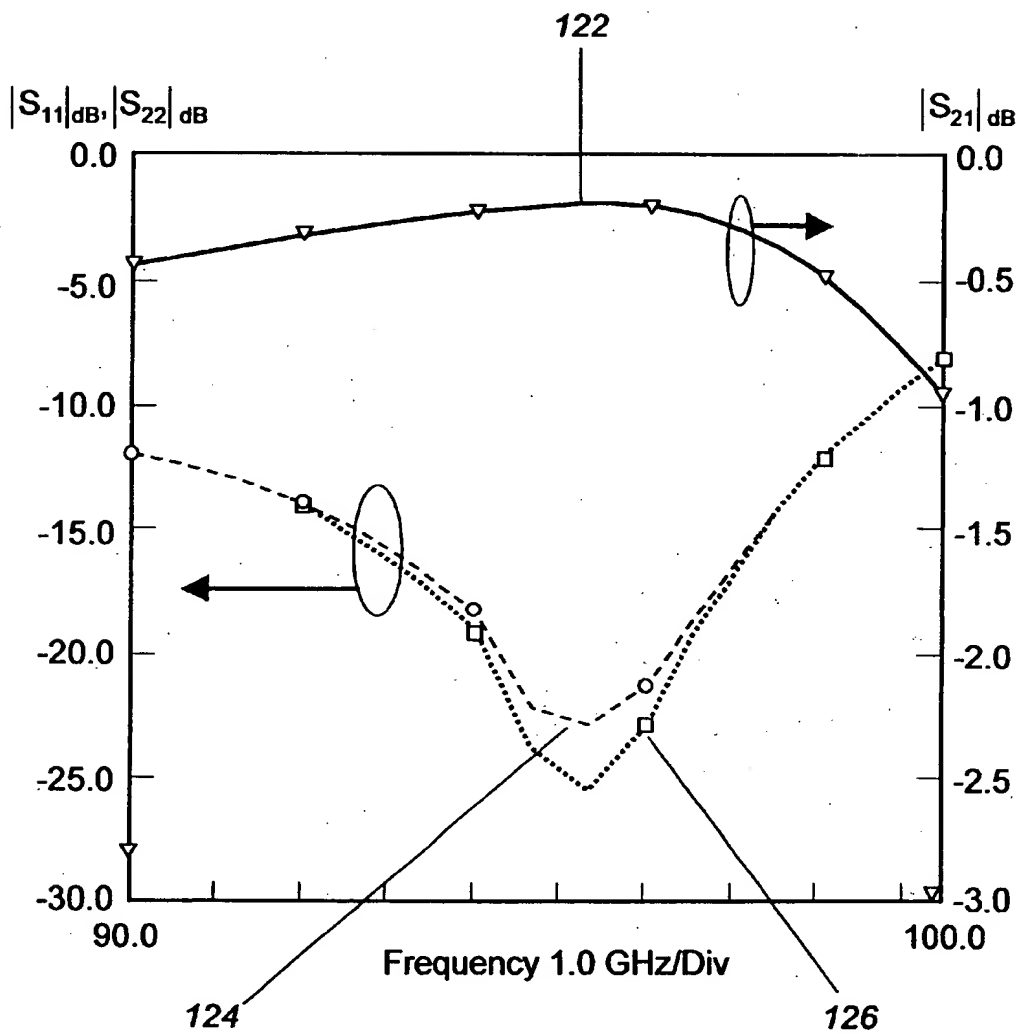
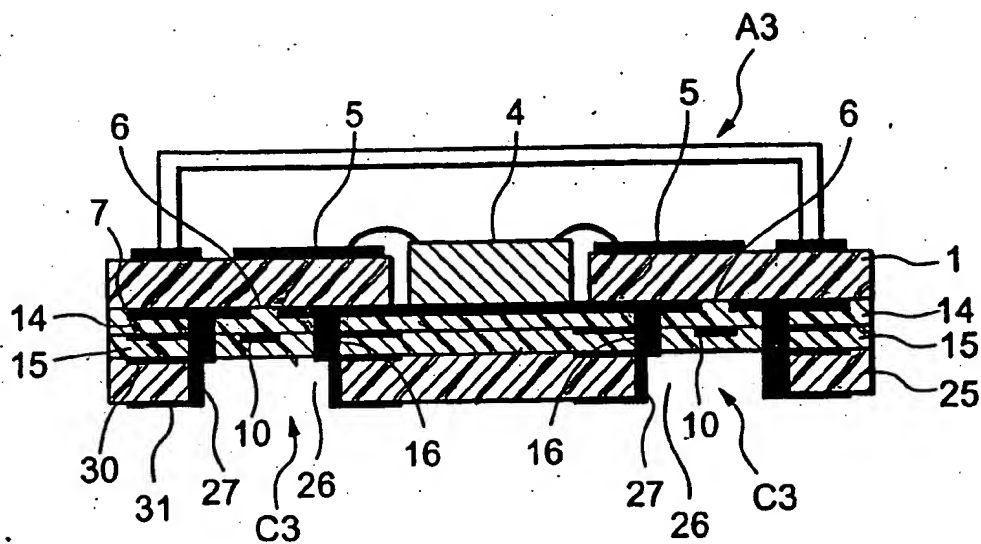


Figure 8



FIG.5



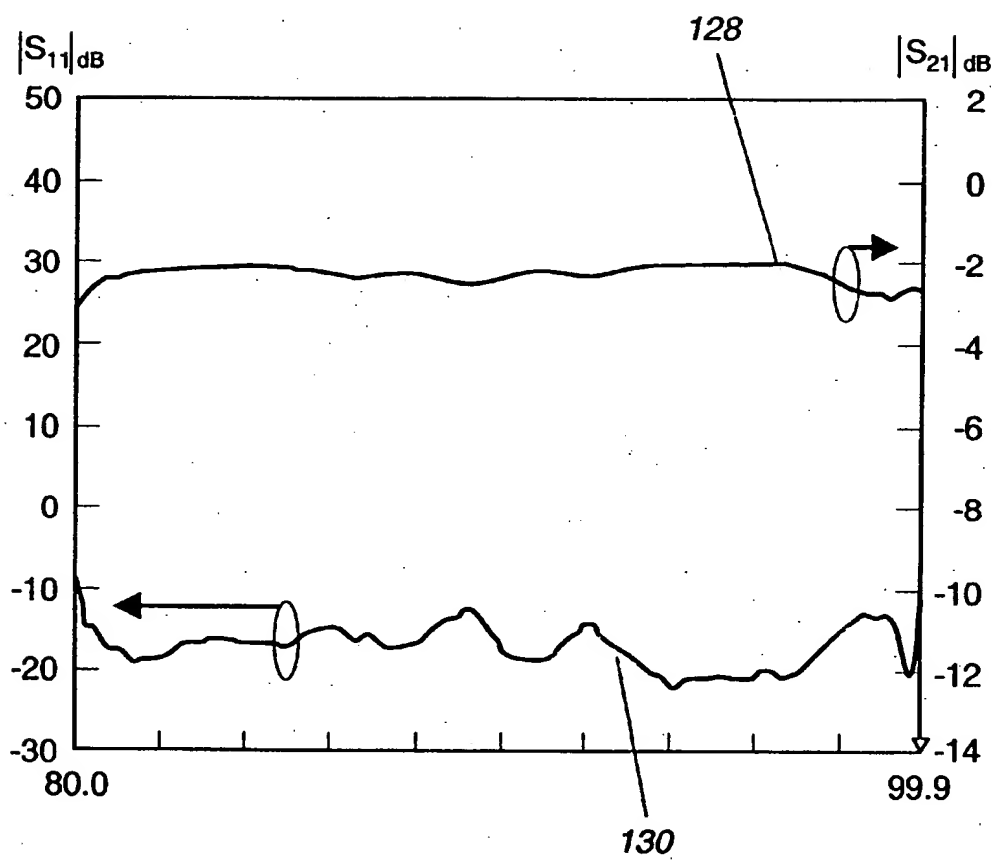


Figure 9





FIG.6a

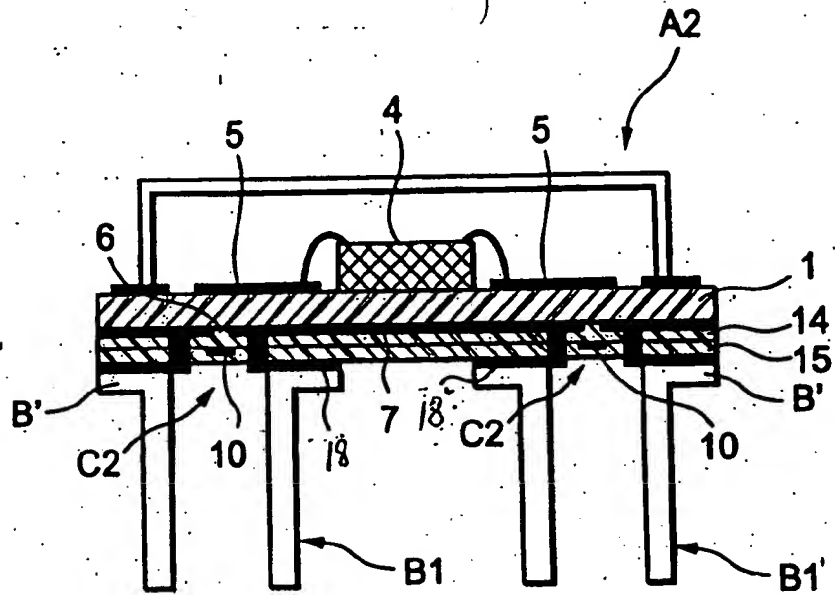


FIG.6b

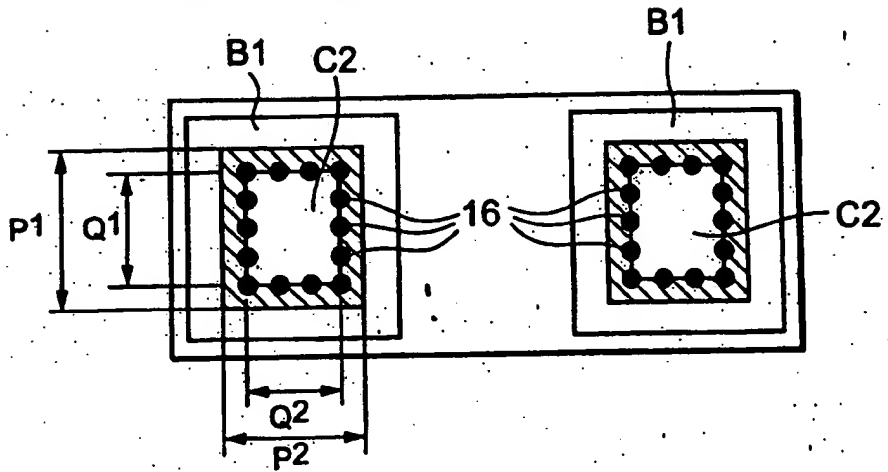
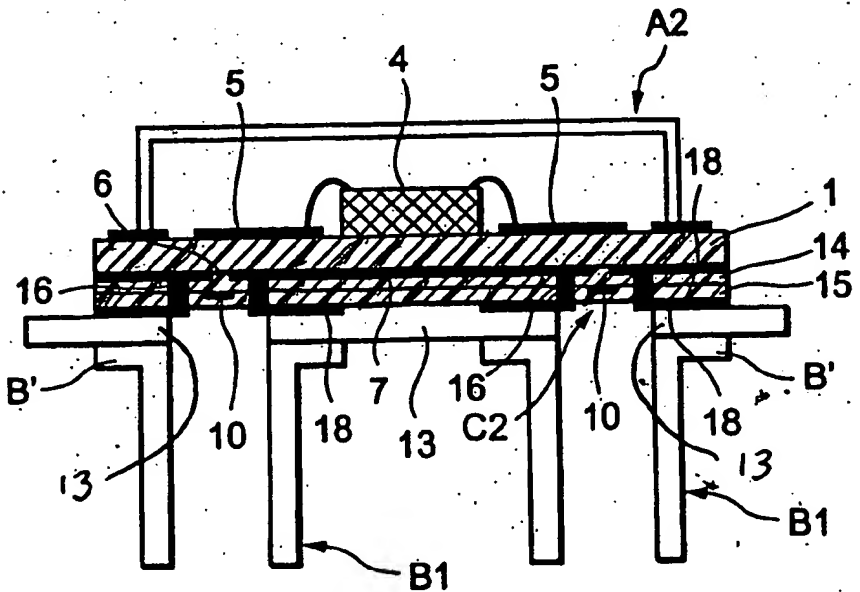
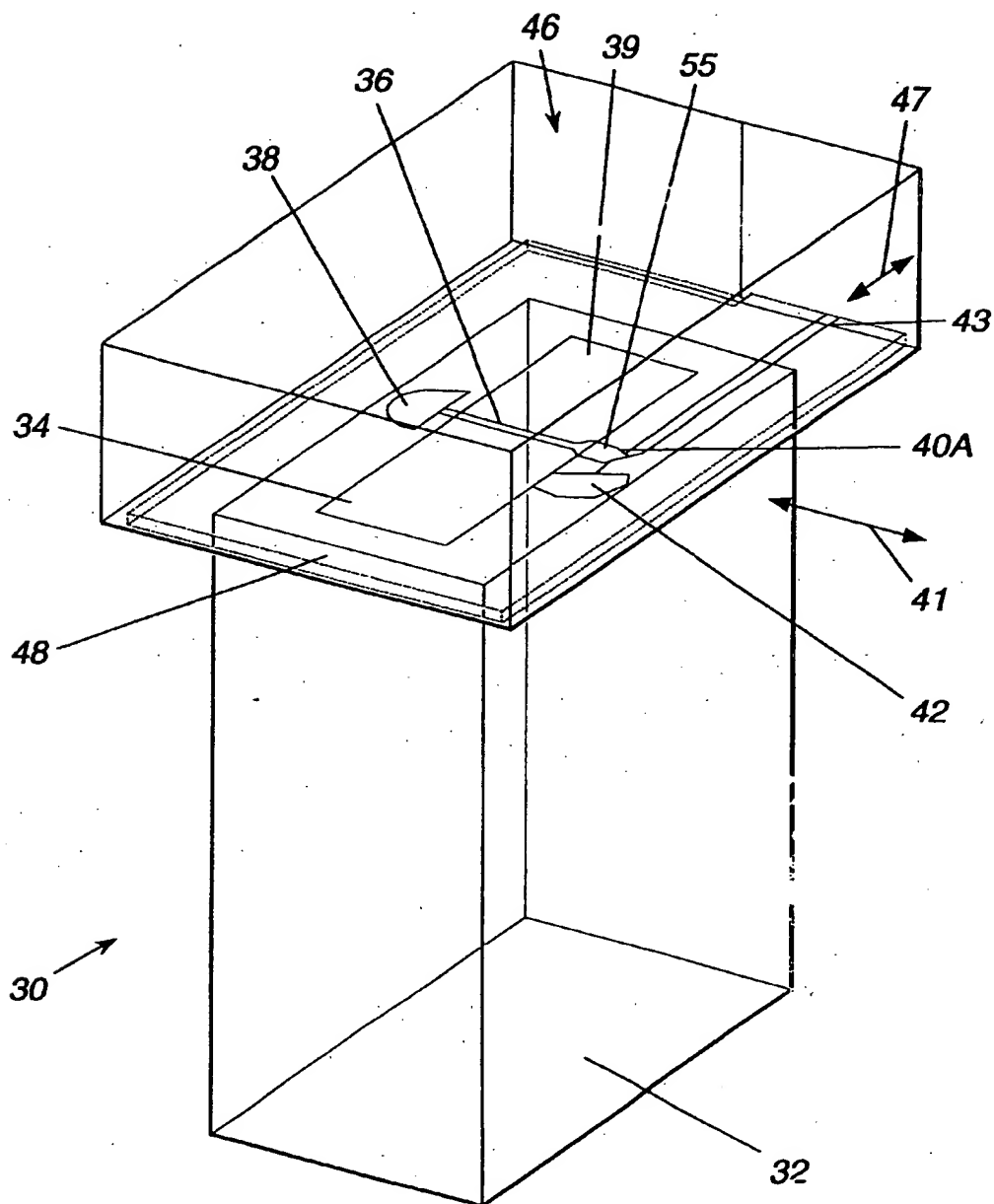


FIG.6c





Figur 10



FIG.7

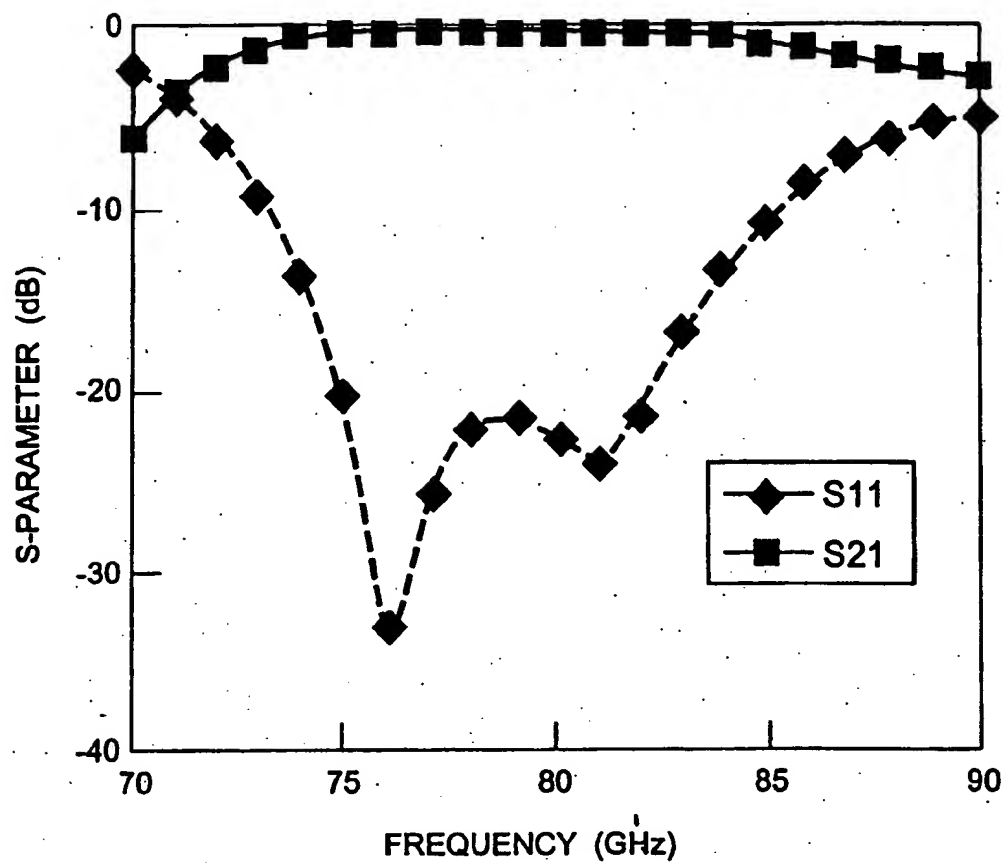
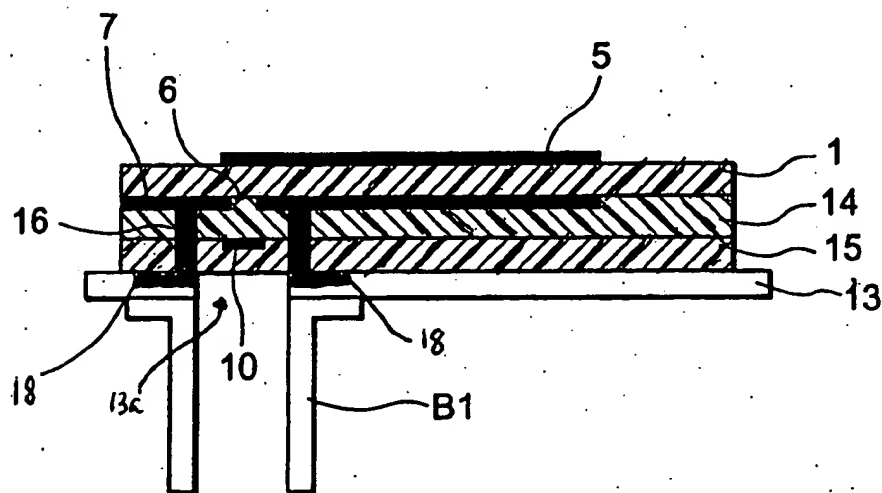


FIG.8



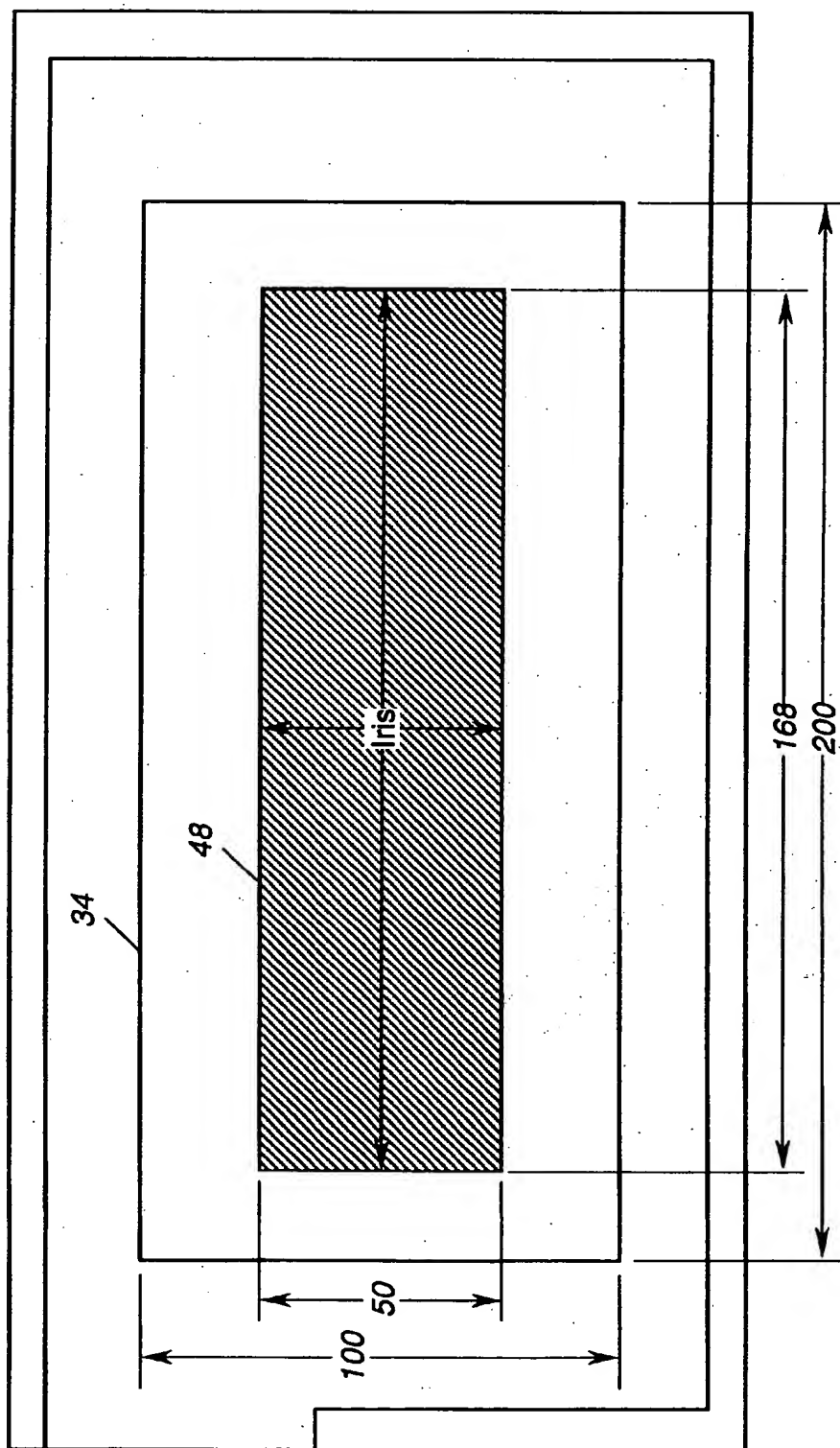


Figure 11